Application No.: 09/835170 Docket No.: SMQ-041/P5213

REMARKS

Claims 1-6, and 24-29 were presented for examination. Claims 1 and 24 were rejected under 35 U.S.C. §102 (b) as anticipated by U.S. Patent No. 5,854,801 to Yamada et al. ("Yamada"). Claims 2-6 and 25-29 were rejected under 35 U.S.C. §103 (a) as obvious over Yamada. Upon entry of this paper, no amendment is made. No new matter is added. Claims 1-6, and 24-29 are presented for examination.

Rejections of claims 1 and 24 under 35 U.S.C. §102 (b)

Independent claim 1 recites an integrated circuit that includes a memory array, a test generator and a conversion circuit. Independent claim 24 recites a semiconductor device that includes a memory array, a test generator and a conversion circuit. Examiner stated that the limitations of "integrated circuit" and "semiconductor device" only appear in the preamble and do not further limit the claim language, and therefore are not considered. Applicant respectfully submits that the Examiner does not interpret the rules of MPEP appropriately. The preamble of "integrated circuit" is not reciting purpose or intended use, but rather states the structure and scope of the invention, and therefore should be considered as a limitation. MPEP 2111.02 specifically points out that any terminology in the preamble that limits the structure of the claimed invention must be treated as a claim limitation.

The claimed invention relates to build-in self-test (BIST) for testing embedded memory because external testing of the embedded memory is difficult due to the lack of direct connection between the input pins, output pins, and the embedded memory of the device. Yamada discusses a test pattern generation apparatus and method to improve the conventional technology of testing semiconductor devices using semiconductor test systems (see Background Art). Therefore, Yamada discusses an improvement of external test systems for testing semiconductor devices, which is very different from scope of the claimed invention.

Furthermore, Examiner's response to previous amendment points out that "Yamada does not teach that all the elements are not on a integrated circuit and one of ordinary skill in the art would have recognized that testing an SRAM would high likely be done on a integrated circuit or a semiconductor device." Applicant respectfully submits that Examiner's statement shows

that Yamada does not specifically disclose all the elements in independent claims 1 and 24 and only suggests that it is not impossible. It is inappropriate to reject independent claims 1 and 24 under 35 U.S.C. §102. Any speculation as to what Yamada teaches or suggests is inappropriate under 35 U.S.C. §102.

Additionally, independent claims 1 and 24 recite a test generator coupled to the memory array to generate a physical address in the memory array. Examiner suggested Yamada teaches this limitation in Fig. 1. However, a closer look at Fig. 1 of Yamada, pattern generator does not generate a physical address in the memory array. Fig. 1 of Yamada shows that the pattern generator output X0-11, Y0-8, Z0-2, and the data inputted to memory array (20) are only X0-11 and Y0-8. Therefore, Yamada does not disclose a test generator that generates physical address in the memory array, as required by both independent claims 1 and 24.

As set forth above, Applicant respectfully submits that Yamada does not disclose each and every element of independent claims 1 and 24, and requests the Examiner to reconsider and withdraw the rejections of claims 1 and 24.

Rejections of claims 2-6 and 25-29 under 35 U.S.C. §103(a)

Dependent claims 2-6, and 25-29 depends from one of independent claims 1 and 24. Yamada fails to teach or suggest an "integrated circuit" or "semiconductor device" as recited by claims 1 and 24. Yamada further fails to teach or suggest a test generator coupled to the memory array that generates a physical address in the memory array.

The Examiner suggested that since wrap conversion includes a predetermined logic circuit, that would mean that the conversion circuit inherently has to have temporarily storage device, and therefore it would have been obvious for one of ordinary skill in the art to include a memory storage device with the wrap conversion circuitry. Applicant respectfully disagrees.

Yamada gives two examples of the predetermined logic circuit in Fig. 3 and Fig. 4. Furthermore, in col. 2, lines 26-30, lines 37-42, lines 56-60, col. 3 lines 6-11, and col. 4 lines 5-10, and lines 19-24, Yamada shows the different logic expressions of the logic circuit based on different embodiments. All these logic expressions are simple logic expressions that require only

a few wires and a few gates to implement in hardware as illustrated in Fig. 3 and Fig. 4. Therefore, it is not inherent to have any temporary storage device to use with the conversion circuit as suggested by the Examiner. Therefore, it is not obvious for one ordinary skill in the art to add a storage device to Yamada and results in the present invention as claimed in independent claims 1 and 24.

Furthermore, Yamada does not suggest pattern generator can generate physical address of the memory device under test because the pattern generator needs to generate extra bits and data in order for the wrap conversion to generate a wrap address.

As set forth above, Yamada does not teach or suggest the elements of a test generator coupled to the memory array to generate a physical address in the memory array or a conversion circuit including a memory device. Therefore, Yamada does not teach or suggest all the limitations in independent claims 1 and 24.

Dependent claims 2-6, 25-29 depends from one of independent claims 1 and 24, and include all the limitations of their corresponding independent claim. Therefore, Yamada does not teach or suggest all the limitations of claims 2-6, and 25-29. Accordingly, Applicant respectfully requests the Examiner to reconsider and withdraw the rejections of claims 2-6 and 25-29.

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CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this statement. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SMQ-041 from which the undersigned is authorized to draw.

Dated: February 4, 2005

Respectfully submitted,

By _____

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